Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1 and 5 have been amended.

In item 4 of the above-identified Office Action, claims 1 - 6 and 8 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,981,179 to Shigemasa et al ("**SHIGEMASA**") in view of U. S. Patent No. 6,990,607 to Sim et al ("**SIM**"). In item 5 of the Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **SHIGEMASA** in view of **SIM**, and further in view of U. S. Patent Application Publication No. 2002/0066056 to Suzuki et al ("**SUZUKI**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

The instant application discloses a system wherein an integrated module carries out a self-test of an integrated memory, without additional BIST hardware has to be provided for this purpose. The module 1 of Fig. 2 of the instant application, is shown as including a memory 2 and a micro controller 3, which, in a normal operation of the module 1,

controls the memory access to the memory 2 and the external data transfer of the module 1. Parts of the microcontroller 3 include a central processing unit 4 and an internal memory, which can be utilized as a command memory 5 and/or as a defect data memory 6.

As disclosed in the instant application, before the beginning of a test operation, a command sequence for carrying out a test sequence that is executed on the microcontroller is read in from a test system 7 of Fig. 2 of the instant application. As also disclosed in the instant application, the process of loading the command sequence into a command memory 5 is controlled by the CPU 4 of Fig. 2 of the instant application. A test is executed by the CPU 4 from a start address of the internal memory. Accordingly, test data are written to the memory 2 by the CPU 4. The data are read out again from the memory 2 under the control of the CPU 4 and corresponding defect data are stored in the defect data memory 6 under the control of the CPU 4. The defect data stored in the defect data memory 6 are read out to outside the module 1, under the control of the CPU 4, to the test system 7, in order to evaluate the functional testing.

Additionally, the specification of the instant application discloses that, on the basis of the defect data, it is

possible to construct a fail bit map for defect analysis purposes of the memory 2 including memory cells for storing data. Then, in order to repair defective memory cells, the memory 2 of Fig. 2 of the instant application also contains **redundant memory cells which are combined to form redundant row lines or redundant column lines.** See, for example, page 2 of the instant application, lines 1 - 5.

As further disclosed in the instant application, during the functional testing, the addresses of the tested memory cells which have been detected as defective are stored in the defect data memory 6 and are read-out under control of the microcontroller, **to outside of the integrated module.** The instant application and claims require, among other limitations, that the addresses read-out to outside the integrated module are evaluated by the test system to calculate a repair solution. On the basis of the repair solution calculated, regular lines having defective memory cells are replaced by the redundant row lines or redundant column lines of the memory 2. See, for example, page 2 of the instant application, lines 1 - 5, which state:

> Integrated memories generally have **redundant memory cells** for repairing defective memory cells, **the redundant memory cells usually being combined to form redundant row lines or redundant column lines which can replace regular lines having defective memory cells** in address terms. [emphasis added by Applicants[

See also, for example, page 2 of the instant application, lines 15 - 23, which state:

> To that end, the addresses of the tested memory cells which have been detected as defective are stored in a defect address memory to form a so-called defect table in order to replace the memory cells by defect-free redundant memory cells in a subsequent step on the basis of the stored addresses. **On the basis of the defect table, the repair solution specific to each memory can subsequently be calculated and a so-called fail bit map can be produced.** [emphasis added by Applicants]

In view of the foregoing disclosure in the specification of the instant application, Applicants have amended claim 1 to recite, among other limitations:

> **a memory including memory cells and redundant memory cells** for storing code and data, **said redundant memory cells being combined to form redundant row lines or redundant column lines;**
>
> . . .
>
> a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller, **said addresses further being read out under control of said microcontroller, to outside of the integrated module, and used to calculate a repair solution to replace regular lines having defective memory cells with the redundant row lines or redundant column lines.** [emphasis added by Applicants]

Similarly, Applicants have amended independent claim 5 to recite, among other limitations:

> A method for functionally checking a memory **including memory cells and redundant memory cells** of an integrated module, which comprises the steps of:
>
> . . .
>
> **using the read-out addresses of the defective memory cells to calculate a repair solution that replaces regular lines having defective memory cells with redundant row lines or redundant column lines formed by redundant memory cells**. [emphasis added by Applicants]

As such, Applicants' amended claims require, among other limitations, a memory including memory cells **and redundant memory cells, wherein defective memory cell addresses are read to outside the integrated module in order to calculate a repair solution that replaces regular lines having defective memory cells with redundant row lines or redundant column lines formed by the redundant memory cells**. None of the cited prior art references, taken alone, or in combination, teach or suggest all limitations of Applicants' presently amended claims.

More particularly, the **SHIGEMASA** reference discloses a microcomputer having a built-in non-volatile memory, and a test system thereof. **SHIGEMASA** discloses transferring a test program from an external communication device to a built-in RAM (12 of Fig. 1 of **SHIGEMASA**), after which the control of a CPU is switched to the built-in RAM to conduct a test on the nonvolatile memory. See, for example, the Abstract of

SHIGEMASA. As such, **SHIGEMASA** clearly discloses **transferring a test program from an external device to the RAM of the microcomputer**. Thus, once the test program is completely transferred **to the built-in RAM of the microcomputer** of **SHIGEMASA**, the CPU 13 of Fig. 1 of **SHIGEMASA**, (which is also in the same microcomputer 11 of **SHIGEMASA**), under control of the test program in the local RAM, runs the test program on the non-volatile memory 11 of **SHIGEMASA**, and creates test result data including the test result. See, for example, col. 7 of **SHIGEMASA**, lines 30 - 39. **SHIGEMASA** discloses that the test on the non-volatile memory 11 is complete when a control computer (30 of Fig. 1 of **SHIGEMASA**) receives a pass/fail judgment from the microcomputer 10 of Fig. 1 of **SHIGEMASA**. See, for example, col. 7 of **SHIGEMASA**, lines 49 - 51.

As such, in contrast to the Applicants' presently claimed invention, the CPU 13 of the microcomputer 10 of the **SHIGEMASA** reference **does not read-out a set of address data of defective memory cells to an external test system to calculate a repair solution that replaces defective memory cells with redundant memory cells**. Rather, the cited **SHIGEMASA** reference discloses that the control computer 30 (i.e., an external device) either receives a pass/fail judgment from the microcomputer 10 or **makes a pass/fail judgment** based on the received memory test result data. See, for example, col. 7 of **SHIGEMASA**, lines 52

- 56. Rather, in **SHIGEMASA**, the memory test result data is read-out to an external device (the computer 30) **solely for the purpose of making a pass/fail judgment, and not to calculate a repair solution that replaces defective memory cells with redundant memory cells.** As such, among other limitations of Applicants' claims, the control computer 30 of **SHIGEMASA does not calculate a repair solution to replace defective memory cells in the non-volatile memory 11 by redundant memory cells**, as required by Applicants' claims.

The **SIM** reference, cited in the Office Action in connection with **SHIGEMASA**, also fails to teach or suggest, among other limitations of Applicants' claims, reading out defective memory cell addresses **to outside the integrated module in order to calculate a repair solution that replaces regular lines having defective memory cells with redundant row lines or redundant column lines formed by the redundant memory cells**. More particularly, the **SIM** reference discloses a system and method for adaptive storage and caching of a defect table. However, in contrast to Applicants' presently claimed invention, the defect table of **SIM** does not contain addresses of memory cells, i.e., addresses arranged between row lines and column lines of a memory. Rather, in **SIM**, the defect table contains information concerning the head, cylinder and sector of the defect location in the mass storage device,

which is formed as a disk drive. See, for example, col. 1, line 64 - col. 2, line 3, which states:

> Where the mass storage device is a disc drive, during operation of disc drive, for every disc access, the target address is expressed as logical block address (LBA). **The LBA is converted to a physical address expressed as a physical cylinder/head/sector (PCHS) address** based on the physical layout of the drive and the information in the defect table. [emphasis added by Applicants]

As such, like **SHIGEMASA**, the **SIM** reference fails to teach or suggest, among other limitations of Applicants' claims, reading-out defective memory addresses to outside of the integrated module to calculate a repair solution to replace defective memory cells of a memory by redundant memory cells, wherein the redundant memory cells are combined to form redundant row lines or redundant column lines. Thus, in Applicants' claimed invention, regular lines having defective memory cells are replaced by **redundant row lines or redundant column lines based on a repair solution calculated from the addresses of defective memory cells.** Such limitation, among others, is neither taught, nor suggested, in the **SIM** reference.

The **SUZUKI** reference, cited in the Office Action in combination with **SHIGEMASA** and **SIM** against Applicants' dependent claim 7, does not cure the above-discussed deficiencies of the **SHIGEMASA** and **SIM** references. As such,

Applicants' claims are believed to be patentable over **SHIGEMASA**, **SUZUKI** and **SIM**, whether taken alone, or in combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5.

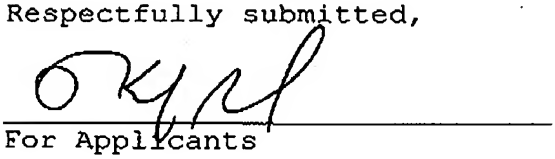
In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

The instant response is being filed simultaneously with a Request for Continuing Examination and its associated fee. If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any additional fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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